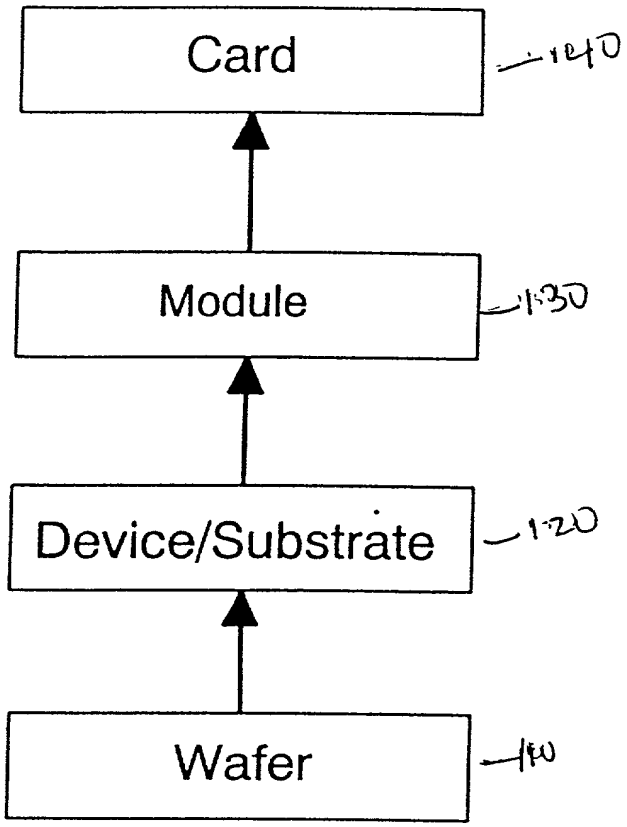


FIGURE 1

09654850.062504

TD9290"05BT6860

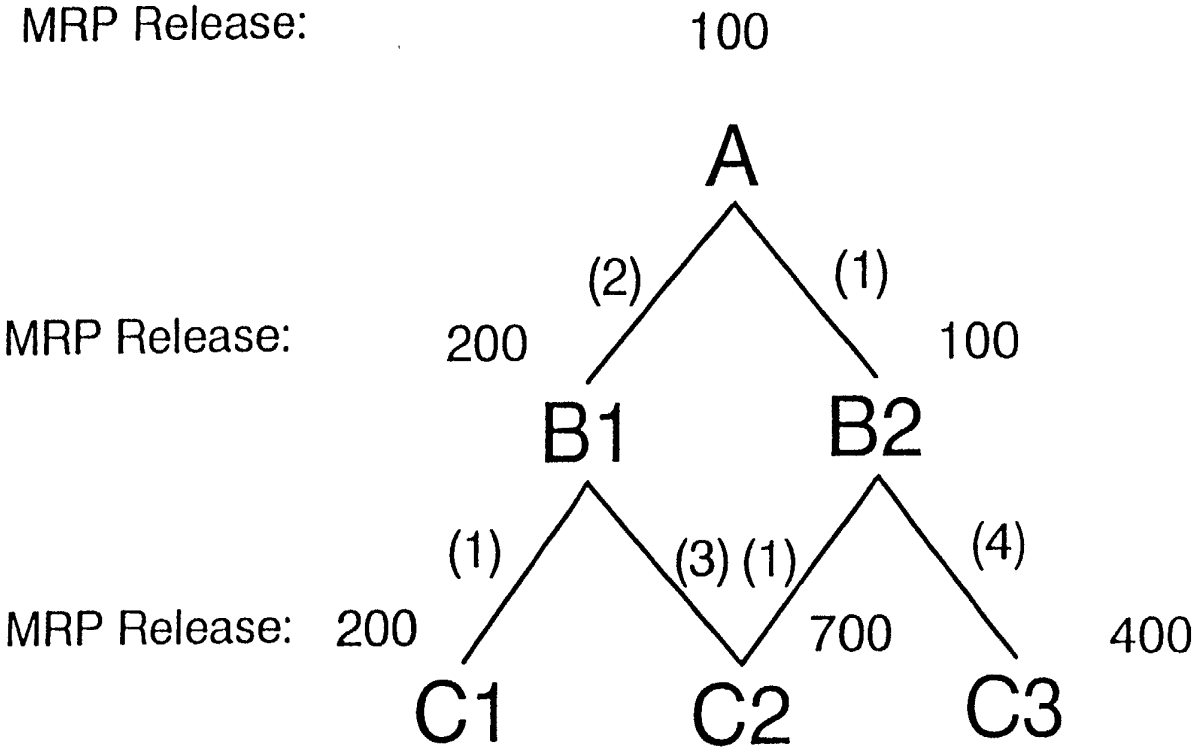


Figure 2

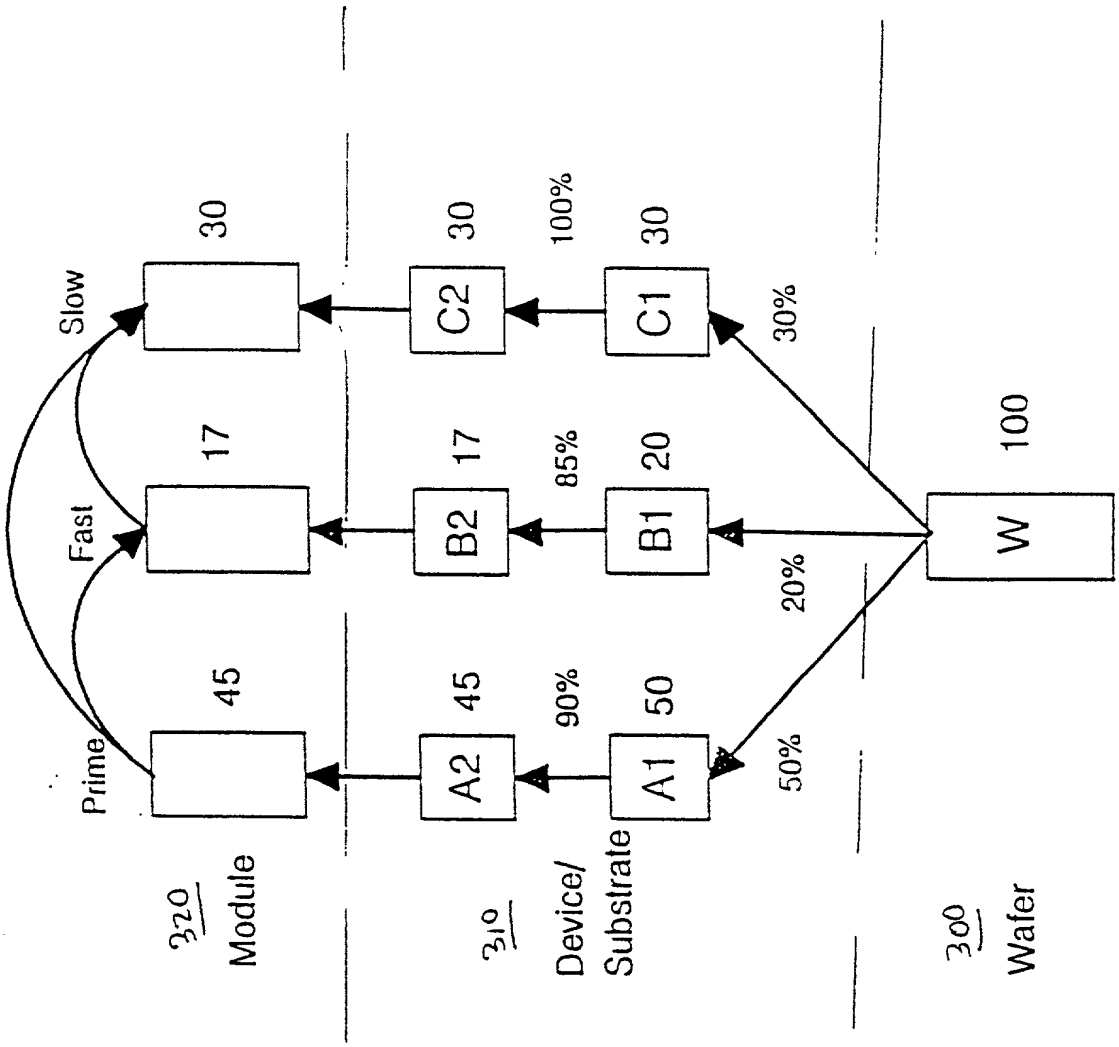
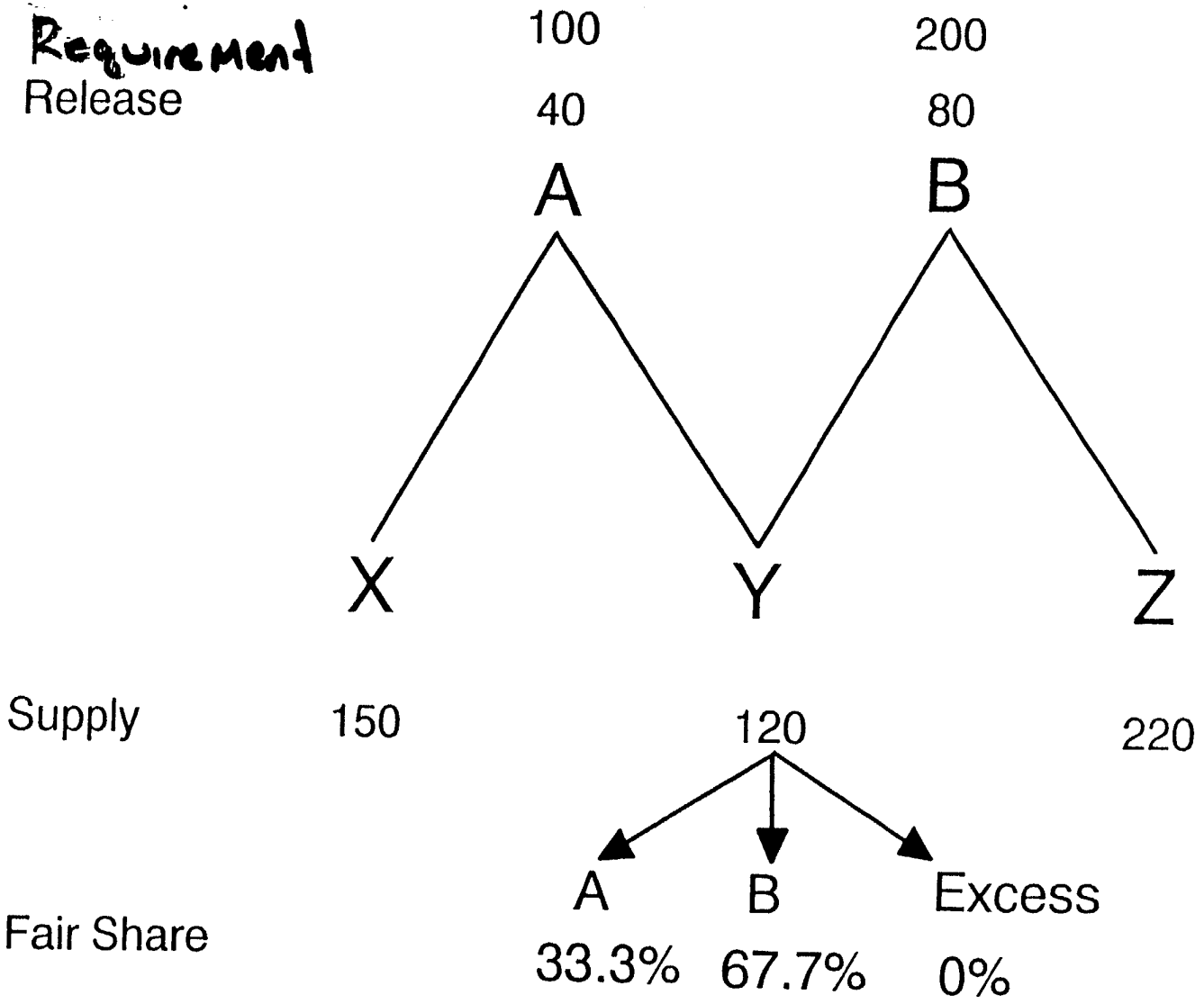

Slow
Fast
Prime
45
17
30
A2
45
B2
17
C2
30
90%
85%
100%
A1
50
B1
20
C1
30
50%
20%
30%
W
100
320
Module
310
Device/
Substrate
300
Wafer

Figure 3


Requirement
Release
100
200
40
80
A
B
X
Y
Z
Supply
150
120
220
A
B
Excess
Fair Share
33.3%
67.7%
0%

Figur 4

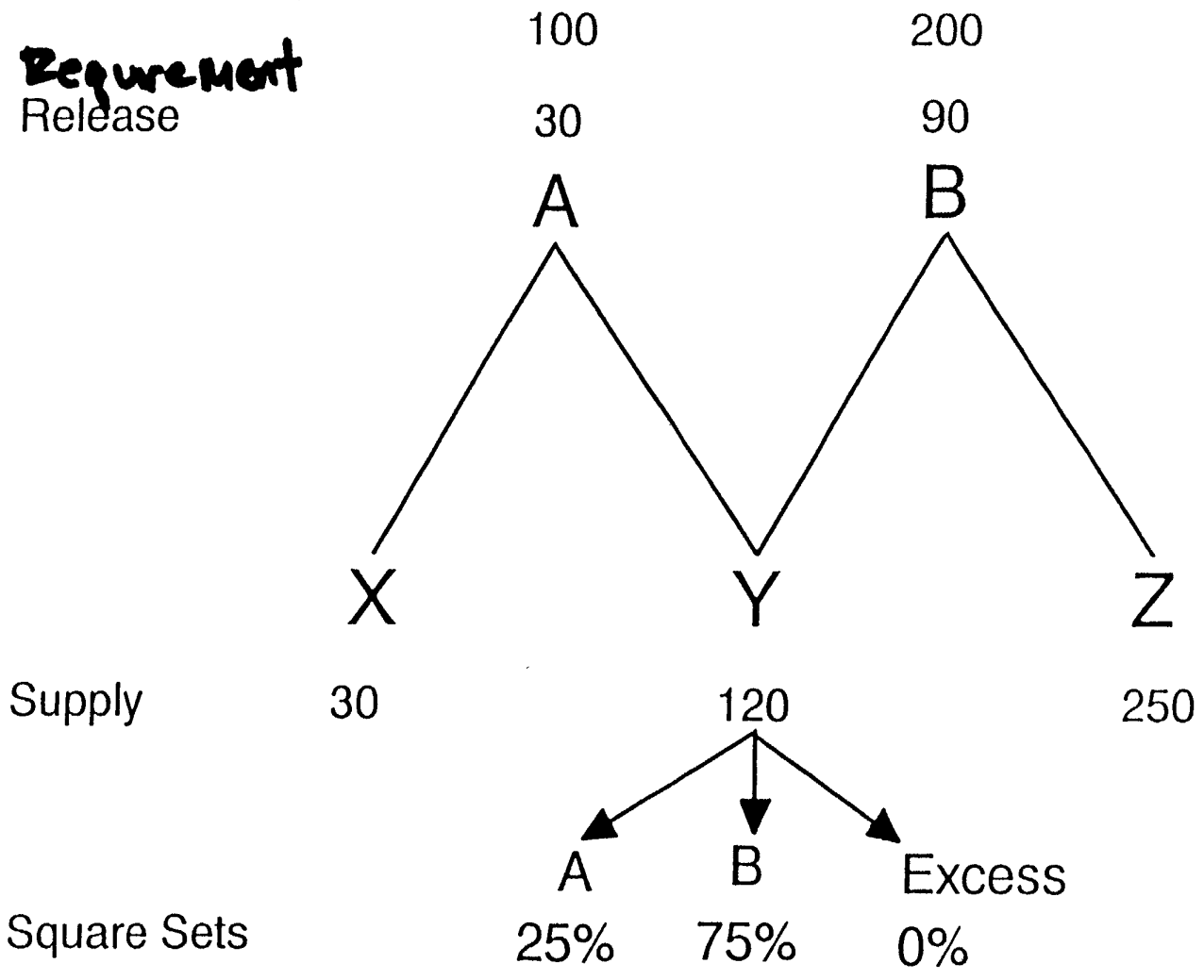

Requirement
Release
100
200
30
90
A
B
X
Y
Z
Supply
30
120
250
A
B
Excess
Square Sets
25%
75%
0%

Figure 5

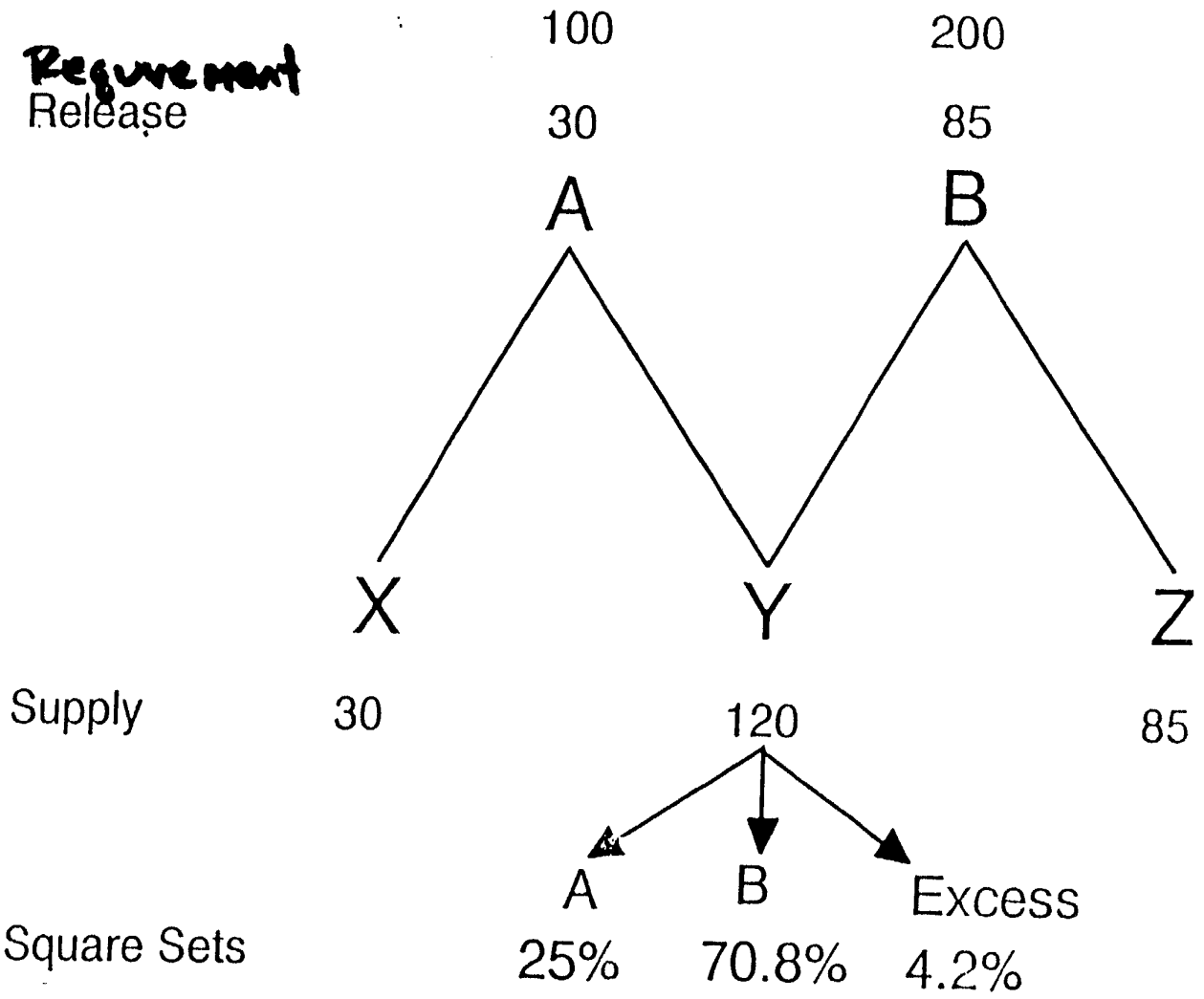

Requirement
Release
100
200
30
85
A
B
X
Y
Z
Supply
30
120
85
A
B
Excess
Square Sets
25%
70.8%
4.2%

Figure 6

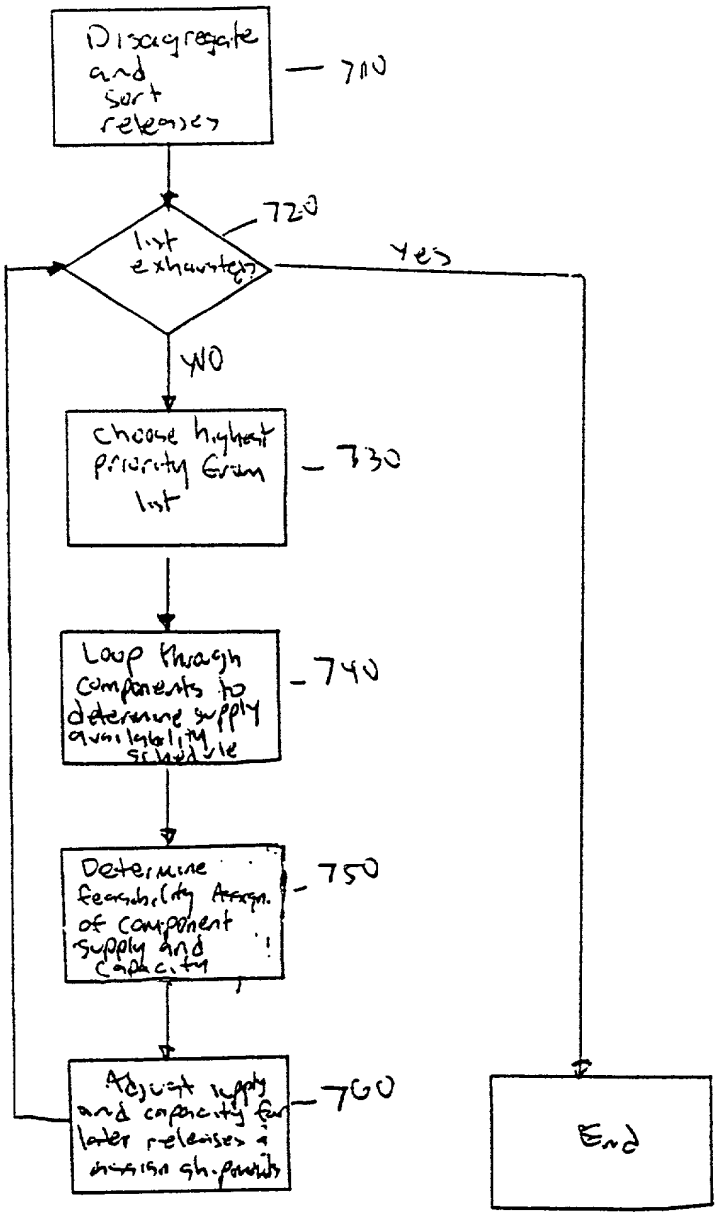

Disaggregate and sort releases
710
720
list exhausted?
Yes
NO
Choose highest priority Gram list
730
Loop through components to determine supply availability schedule
740
Determine feasibility Assign. of component supply and capacity
750
Adjust supply and capacity for later releases a
760
End

FIGURE 7.

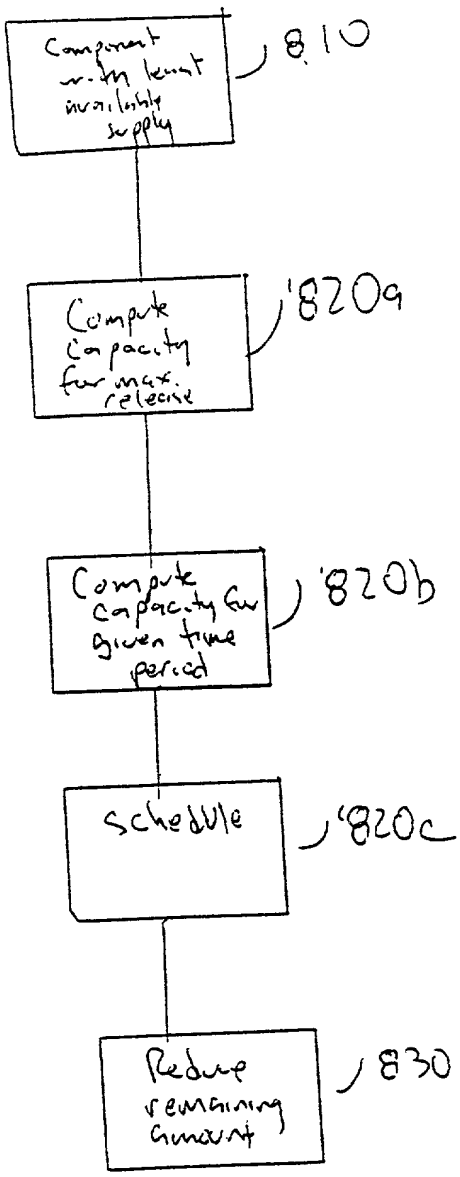


Figure 8

09525850 - 052505

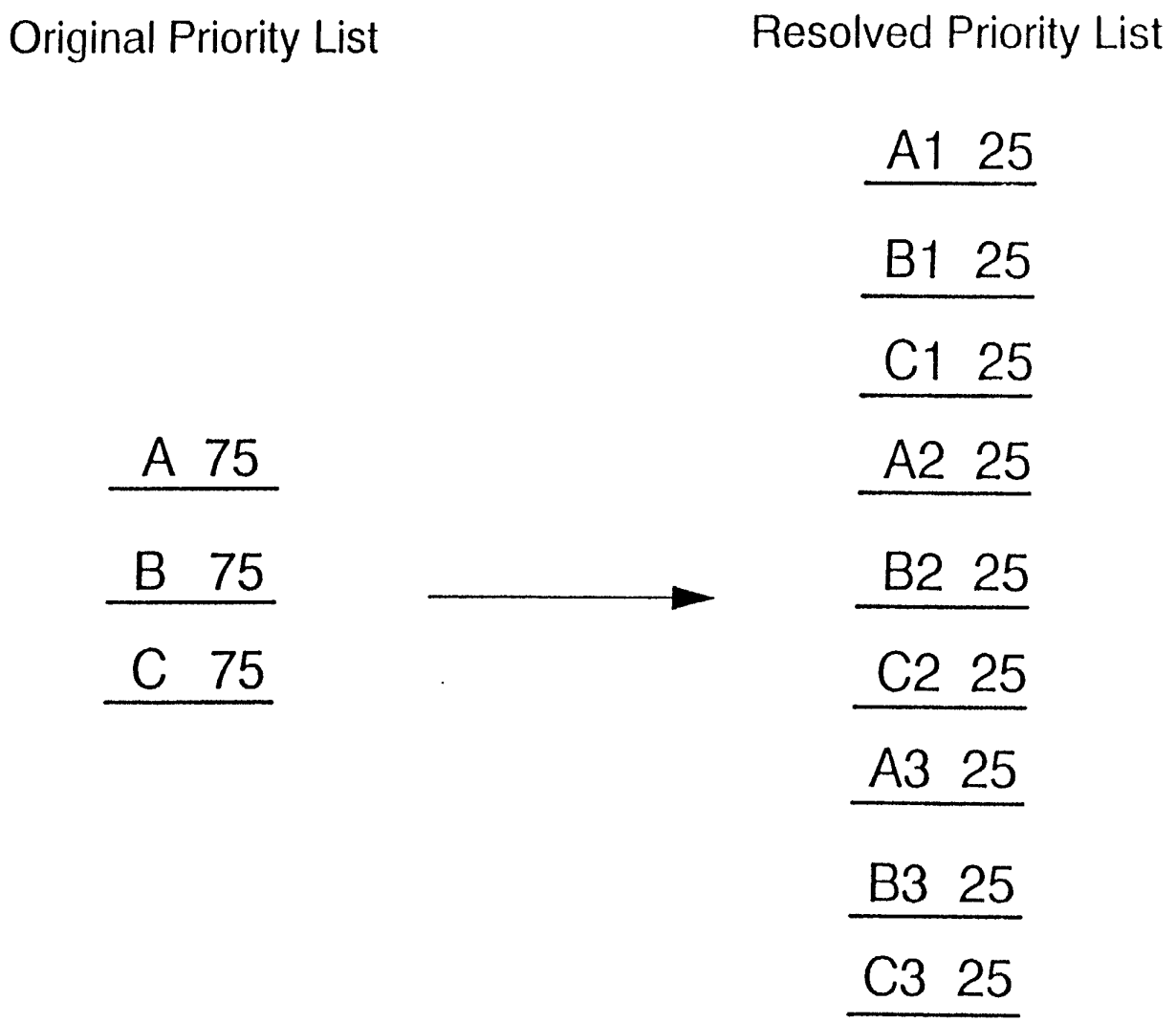

Original Priority List
Resolved Priority List
A 75
B 75
C 75
A1 25
B1 25
C1 25
A2 25
B2 25
C2 25
A3 25
B3 25
C3 25

Figure 9